

## PATENT ABSTRACTS OF JAPAN

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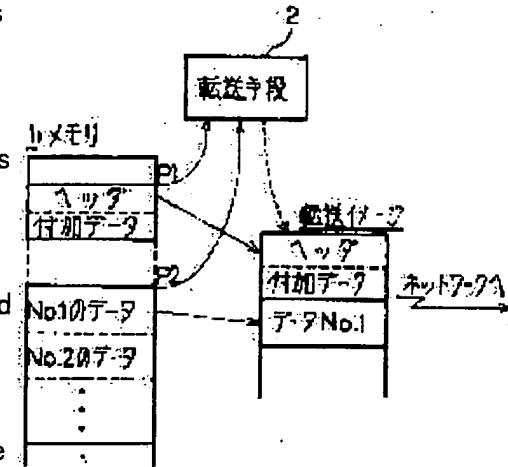
(72)Inventor : NISHIKAWA KATSUHIKO

## (54) DATA TRANSFER SYSTEM

## (57)Abstract:

PURPOSE: To eliminate unnecessary reading from and writing to a memory and to improve transfer speed by previously generating a header by writing dummy data so as to make an integral multiple of the number at the tail of 1st data.

CONSTITUTION: A transfer means 2 informed of the head address P1 of a header in a memory 1 and the head address of data reads the header and additional data (dummy data), written previously to an integral multiple of some number, out of the address P1 and transfers them to a network. Then the data are read out in blocks from the reported head address P2 of the data in the memory 1 while sectioned to an integral multiple of the certain number, and transferred to the network. Those are repeated to the end of the data. It is not necessary to read and write the data out and in the memory 1 to make blocks the integral multiple of the certain number like before, and the data can be transferred fast.



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**CLAIMS**

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**[Claim(s)]**

[Claim 1] In a data transfer system which makes data an integral multiple of a certain number, chains it, and transmits it, Dummy data is beforehand added so that it may become a number of integral multiples which have the 1st data concerned in the rear of the 1st data, A data transfer system provided with a means to divide into an integral multiple of a certain number the 1st data in which dummy data of a number of integral multiples which exist at the time of transmission was added, and the 2nd data, to chain them, and to transmit them.

[Claim 2] The data transfer system according to claim 1 adding data length which it is going to transmit in the above-mentioned dummy data.

[Claim 3] Claim 1 using the 1st data of the above as data which is going to transmit a header and the 2nd data, or the data transfer system according to claim 2.

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**DETAILED DESCRIPTION****[Detailed Description of the Invention]****[0001]**

[Industrial Application] This invention makes data the integral multiple of a certain number, and relates to the data transfer system chained and transmitted.

[0002] When transmitting the data stored in external storages, such as a hard disk, via a network, it is necessary to add a header to the head of data and to perform chaining. In the interface chip etc. of the network in which such chaining is possible, there may be restriction of not operating unless it is a number with the length of the data chained of integral multiples. When there is this restriction, to perform chaining of a header and data simply and promptly is desired.

**[0003]**

[Description of the Prior Art] The situation of the conventional chaining is shown in drawing 4. Drawing 4 shows the explanatory view of conventional technology.

[0004] First, the data on the disk unit which is an external storage once reads continuously like \*\* of the memory 21, and stores. Then, read the header currently beforehand written in the portion of \*\* of the memory 21 for every transfer unit, and it writes in the portion of \*\* of other memories 21. A part of data No.1 in a figure is written in so that the data of the portion of \*\* may be read and it may become an integral multiple of a certain number (for example, 48 bytes) exactly after this. And he divides and carries out chaining and was trying to transmit a header and the remaining data so that it may become an integral multiple of a certain number.

**[0005]**

[Problem(s) to be Solved by the Invention] For this reason, when creating the header of the integral multiple of a certain number, read a header and write in on other memories, and read from the head of data after this and it writes in. Since the remaining data was divided into the integral multiple of a certain number, chaining was carried out to this created header and it had transmitted via the network, after considering it as the integral multiple of a certain number exactly and creating a header. In order to create a header, read-out and writing occur within a memory, moreover it is necessary to divide into the integral multiple of the remaining numbers of data \*\*\*\*, and to perform chaining each time, reading and writing of an excessive memory, etc. occur, and there is a problem of reducing a transfer rate.

[0006] This invention writes in dummy data and creates the header beforehand so that it may become a number at the rear of the 1st data (for example, header) of integral multiples, in order to solve these problems. Chaining of this 1st data and the 2nd data that should be transmitted is carried out, it is transmitted, generating of excessive reading and writing is lost within a memory, and it aims at aiming at improvement in a transfer rate.

**[0007]**

[Means for Solving the Problem] With reference to drawing 1, The means for solving a technical problem is explained. In drawing 1, the memory 1 stores a header, data, etc. which it is going to

transmit.

[0008]The transfer means 2 takes out a header and data from the memory 1, and transmits them to an address via a network.

[0009]

[Function]This invention corresponds to the notice of the start address P2 of the data which is the start address P1 and the 2nd data of a header which are the 1st data and which it is going to transmit, as shown in drawing 1. Transmit collectively the dummy data added beforehand to a network as a block so that the transfer means 2 may serve as an integral multiple of a header and a certain number from the start address P1, and He divides into a block and is trying to transmit to a network so that it may become an integral multiple of a certain number from the start address P2 continuously.

[0010]Under the present circumstances, he adds the data length which it is going to transmit to the dummy data in a header, and is trying to transmit. He uses the 1st data as the data which is going to transmit a header and the 2nd data, and is trying to transmit it.

[0011]Therefore, write in DAMIDETA and it creates beforehand so that it may become a number which is the 1st data of integral multiples which are in the rear of a header, for example, By dividing and carrying out chaining and transmitting this 1st data and the 2nd data that should be transmitted so that it may become an integral multiple of a certain number, generating of excessive reading and writing etc. is lost within the conventional memory, and it becomes possible to raise a transfer rate.

[0012]

[Example]Next, the composition and operation of the example of this invention are explained to details one by one using drawing 3 from drawing 1.

[0013]Drawing 1 shows 1 example lineblock diagram of this invention. In drawing 1, the memory 1 tends to store the data which is the header and the 2nd data which are the 1st data and which it is going to transmit. Here, attached data is added and stored so that it may become a number of predetermined number twice currently continued to a header and this header from the address P1. The data (No.1, No.2 ...) which it is going to transmit from the address P2 is stored in continuation.

[0014]Next, the operation at the time of a data transfer is explained.

(1) The transfer means 2 which received the notice of the start address P1 of the header in the memory 1, and the start address P2 of data, The attached data (dummy data) written in beforehand is read so that it may become an integral multiple of a header and a certain number from the address P1, and it transmits to a network like a graphic display transmission image.

[0015](2) Then, divide so that it may become an integral multiple of a certain number from the start address P2 of the data in the memory 1 which received the notice about data, read as a block, and repeat until data is lost [ transmitting to a network like a graphic display transmission image, and ].

[0016]Since it is beforehand written in so that it may become a number of integral multiples which have attached data following a header and this header by the above, If the notice of the start address P1 of a header and the start address P2 of data is received, the transfer means 2, The block of the integral multiple of a certain number is then used like the transmission image of a graphic display, it can transmit to a network one by one, the reading and writing for using the block of the integral multiple of the number which is in the conventional memory 1 become unnecessary, and it becomes possible to carry out data transfer at high speed.

[0017]Drawing 2 shows the system block figure of this invention. In drawing 2, the external storages 11 are external storages, such as a magnetic disk drive, and store the data which it is going to transmit to a network.

[0018]The data I/O part 12 writes in attached data into the memory 1 so that it may indicate to drawing 3 mentioned later and may become a number of integral multiples currently continued to the header generated by the header generating part 16, and this header, or, The data read from the external storage 11 is written in the continuation field in the memory 1.

[0019]The transmission section 13 reads a header and data from the memory 1 to every block (data

divided into the integral multiple of a certain number), and transmits to a network. The network 14 is a net which transmits the data (a packet, a frame, etc.) transmitted from the transmission section 13 to an address.

[0020]The receive section 15 receives the header and data which have been transmitted via the network 14, takes out data, and hands an application program etc. Next, according to the turn of the explanatory view of drawing 3, operation of the composition of drawing 1 and drawing 2 is explained in detail.

[0021] Drawing 3 shows the explanatory view of this invention of operation. Here, the data I/O part 12, the transmission section 13, the receive section 15, and the header generating part 16 are the same as that of the thing of the same number of drawing 2.

[0022] In drawing 3, S1 generates a header. S2 adds data length. Exactly, this adds attached data to the header generated by S1 so that it may become an integral multiple of a certain number (for example, 48 bytes).

[0023]S3 is written in a memory. This is written in like a graphic display of the header and attached data which made what made the header and attached data which were created by S1 and S2 the integral multiple of a certain number a number of integral multiples which are, for example in the memory 1 of drawing 1.

[0024]S4 reads data. This reads the data which it is going to transmit from the external storage 11. S5 is written in a memory. This writes the data read from the external storage 11 by S4 one by one like "the data of No.1", and "the data of No.2", for example in the continuous field in the memory 1 of drawing 1.

[0025]S6 notifies the pointer of a header unit. This notifies the transmission section 13 of the start address P1 of the header written in the memory 1 by S3, and attached data. S7 notifies the pointer of a data division. This notifies the transmission section 13 of the start address P2 of the data written in the memory 1 by S5.

[0026]When the data transfer directions specified as the address as which the data I/O part 12 was specified by the above are received, Add attached data and it writes in the memory 1 so that it may become a number in the header which consists of an address etc. which the header generating part 16 generated, and which were specified of integral multiples, and the data specified from the external storage 11 is read, and it writes in the memory 1. And the transmission section 13 is notified of the start address P1 of a header and attached data, and the start address P2 of data, and a transmission request is carried out. It means that the number of times of reading and writing is made into the minimum, and is written in on the memory 1 by these based on the header and data which were read from the external storage 11, and transmitting preparation was completed.

[0027]S8, the transmission section 13 transmits a header/data. This transmits a header (header + attached data) and data to a network one by one, respectively from the pointer (start address P1) of a header unit and the pointer (start address P2) of a data division which received the notice by S6 and S7.

[0028]The receive section 15 receives the header to which S9 was transmitted by S8. S10 receives data. This receives data after having received the header by S9.

[0029]S11 is distinguished in received-data length = data length. This distinguishes whether the received-data length which received is equal to the data length set as the header. Since finishing [ reception of all the data ] was turned out in YES, a series of processings are ended. Since it became clear that there is data which has not yet been received on the other hand in NO, it returns to S10 and data receiving is repeated.

[0030]In this example, although a header and data are stored in the memory 1, it may store in a separate memory.

[0031]

[Effect of the Invention] Attached data is written in so that it may become a number at the rear of the 1st data (for example, header) of integral multiples according to this invention, as explained

above, Since the composition which divides and carries out chaining of this 1st data and the 2nd data that should be transmitted, and transmits it is adopted, generating of excessive reading and writing can be eliminated within the conventional memory, and improvement in a transfer rate can be aimed at.

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**TECHNICAL FIELD**

[Industrial Application] This invention makes data the integral multiple of a certain number, and relates to the data transfer system chained and transmitted.

[0002] When transmitting the data stored in external storages, such as a hard disk, via a network, it is necessary to add a header to the head of data and to perform chaining. In the interface chip etc. of the network in which such chaining is possible, there may be restriction of not operating unless it is a number with the length of the data chained of integral multiples. When there is this restriction, to perform chaining of a header and data simply and promptly is desired.

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**PRIOR ART**

[Description of the Prior Art] The situation of the conventional chaining is shown in drawing 4. Drawing 4 shows the explanatory view of conventional technology.

[0004] First, the data on the disk unit which is an external storage once reads continuously like \*\* of the memory 21, and stores. Then, read the header currently beforehand written in the portion of \*\* of the memory 21 for every transfer unit, and it writes in the portion of \*\* of other memories 21. A part of data No.1 in a figure is written in so that the data of the portion of \*\* may be read and it may become an integral multiple of a certain number (for example, 48 bytes) exactly after this. And he divides and carries out chaining and was trying to transmit a header and the remaining data so that it may become an integral multiple of a certain number.

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**EFFECT OF THE INVENTION**

[Effect of the Invention]Attached data is written in so that it may become a number at the rear of the 1st data (for example, header) of integral multiples according to this invention, as explained above. Since the composition which divides and carries out chaining of this 1st data and the 2nd data that should be transmitted, and transmits it is adopted, generating of excessive reading and writing can be eliminated within the conventional memory, and improvement in a transfer rate can be aimed at.

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**TECHNICAL PROBLEM**

[Problem(s) to be Solved by the Invention] For this reason, when creating the header of the integral multiple of a certain number, read a header and write in on other memories, and read from the head of data after this and it writes in. Since the remaining data was divided into the integral multiple of a certain number, chaining was carried out to this created header and it had transmitted via the network, after considering it as the integral multiple of a certain number exactly and creating a header. In order to create a header, read-out and writing occur within a memory, moreover it is necessary to divide into the integral multiple of the remaining numbers of data \*\*\*\*, and to perform chaining each time, reading and writing of an excessive memory, etc. occur, and there is a problem of reducing a transfer rate.

[0006] This invention writes in dummy data and creates the header beforehand so that it may become a number at the rear of the 1st data (for example, header) of integral multiples, in order to solve these problems, Chaining of this 1st data and the 2nd data that should be transmitted is carried out, it is transmitted, generating of excessive reading and writing is lost within a memory, and it aims at aiming at improvement in a transfer rate.

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**MEANS**

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[Means for Solving the Problem] With reference to drawing 1, The means for solving a technical problem is explained. In drawing 1, the memory 1 stores a header, data, etc. which it is going to transmit.

[0008] The transfer means 2 takes out a header and data from the memory 1, and transmits them to an address via a network.

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**OPERATION**

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[Function] This invention corresponds to the notice of the start address P2 of the data which is the start address P1 and the 2nd data of a header which are the 1st data and which it is going to transmit, as shown in drawing 1, Transmit collectively the dummy data added beforehand to a network as a block so that the transfer means 2 may serve as an integral multiple of a header and a certain number from the start address P1, and He divides into a block and is trying to transmit to a network so that it may become an integral multiple of a certain number from the start address P2 continuously.

[0010] Under the present circumstances, he adds the data length which it is going to transmit to the dummy data in a header, and is trying to transmit. He uses the 1st data as the data which is going to transmit a header and the 2nd data, and is trying to transmit it.

[0011] Therefore, write in DAMIDETA and it creates beforehand so that it may become a number which is the 1st data of integral multiples which are in the rear of a header, for example, By dividing and carrying out chaining and transmitting this 1st data and the 2nd data that should be transmitted so that it may become an integral multiple of a certain number, generating of excessive reading and writing etc. is lost within the conventional memory, and it becomes possible to raise a transfer rate.

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**EXAMPLE**

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[0013] Drawing 1 shows 1 example lineblock diagram of this invention. In drawing 1, the memory 1 tends to store the data which is the header and the 2nd data which are the 1st data and which it is going to transmit. Here, attached data is added and stored so that it may become a number of predetermined number twice currently continued to a header and this header from the address P1. The data (No.1, No.2---) which it is going to transmit from the address P2 is stored in continuation.

[0014] Next, the operation at the time of a data transfer is explained.

(1) The transfer means 2 which received the notice of the start address P1 of the header in the memory 1, and the start address P2 of data. The attached data (dummy data) written in beforehand is read so that it may become an integral multiple of a header and a certain number from the address P1, and it transmits to a network like a graphic display transmission image.

[0015] (2) Then, divide so that it may become an integral multiple of a certain number from the start address P2 of the data in the memory 1 which received the notice about data, read as a block, and repeat until data is lost [ transmitting to a network like a graphic display transmission image, and ].

[0016] Since it is beforehand written in so that it may become a number of integral multiples which have attached data following a header and this header by the above, If the notice of the start address P1 of a header and the start address P2 of data is received, the transfer means 2, The block of the integral multiple of a certain number is then used like the transmission image of a graphic display, it can transmit to a network one by one, the reading and writing for using the block of the integral multiple of the number which is in the conventional memory 1 become unnecessary, and it becomes possible to carry out data transfer at high speed.

[0017] Drawing 2 shows the system block figure of this invention. In drawing 2, the external storages 11 are external storages, such as a magnetic disk drive, and store the data which it is going to transmit to a network.

[0018] The data I/O part 12 writes in attached data into the memory 1 so that it may indicate to drawing 3 mentioned later and may become a number of integral multiples currently continued to the header generated by the header generating part 16, and this header, or, The data read from the external storage 11 is written in the continuation field in the memory 1.

[0019] The transmission section 13 reads a header and data from the memory 1 to every block (data divided into the integral multiple of a certain number), and transmits to a network. The network 14 is a net which transmits the data (a packet, a frame, etc.) transmitted from the transmission section 13 to an address.

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[0027] S8, the transmission section 13 transmits a header/data. This transmits a header (header + attached data) and data to a network one by one, respectively from the pointer (start address P1) of a header unit and the pointer (start address P2) of a data division which received the notice by S6 and S7.

[0028] The receive section 15 receives the header to which S9 was transmitted by S8. S10 receives data. This receives data after having received the header by S9.

[0029] S11 is distinguished in received-data length = data length. This distinguishes whether the received-data length which received is equal to the data length set as the header. Since finishing [reception of all the data] was turned out in YES, a series of processings are ended. Since it became clear that there is data which has not yet been received on the other hand in NO, it returns to S10 and data receiving is repeated.

[0030] In this example, although a header and data are stored in the memory 1, it may store in a separate memory.

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**DESCRIPTION OF DRAWINGS**

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**[Brief Description of the Drawings]**

[Drawing 1] It is 1 example lineblock diagram of this invention.

[Drawing 2] It is a system block figure of this invention.

[Drawing 3] It is an explanatory view of this invention of operation.

[Drawing 4] It is an explanatory view of conventional technology.

**[Description of Notations]**

- 1: Memory
- 2: Transfer means
- 11: External storage
- 12: Data I/O part
- 13: Transmission section
- 14: Network
- 15: Receive section

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[Translation done.]

## \* NOTICES \*

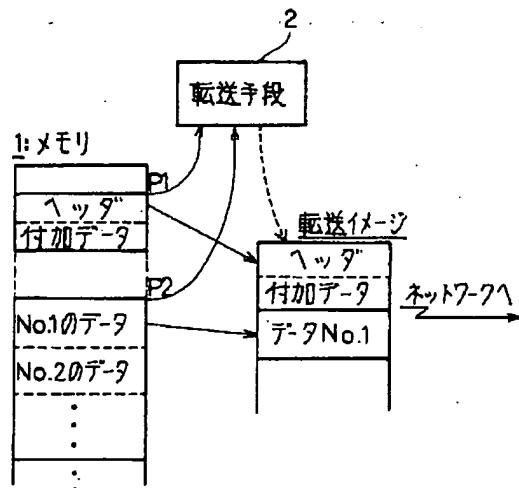
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## DRAWINGS

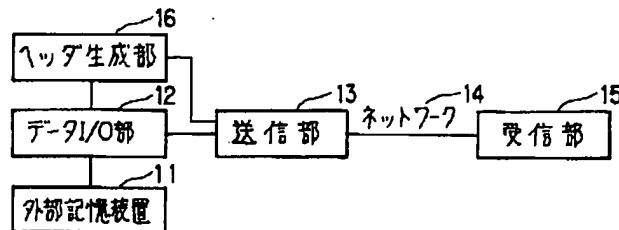
## [Drawing 1]

本発明の1実施例構成図



## [Drawing 2]

本発明のシステムアロット図



## [Drawing 3]